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Media Alert: Cadence to Showcase Signal- and Power-Integrity Solutions at DesignCon 2017

SAN JOSE, Calif., Jan. 27, 2017—Cadence Design Systems, Inc. (NASDAQ: CDNS) today announced plans to showcase its latest Sigrity™ signal and power integrity technologies in booth 515 at DesignCon from January 31 to February 2, 2017, in Santa Clara, Calif. To learn more about the Cadence® activities at DesignCon and to register for the conference, visit https://www.cadence.com/content/cadence-www/global/en_US/home/company/events/industry-events/designcon-2017.html.

WHAT: Cadence experts are scheduled to discuss new developments in these technologies and how they can help solve today's signal integrity challenges during the following speaking sessions:

- **Panel: Getting the Most from IBIS-AMI: Tips and Secrets from the Experts—** Tuesday, January 31 at 4:45 p.m., Ken Willis, product engineering director
- **Team-Based PCB PDN Design Methodology Enabled by IC Target Impedance Constraints—**Wednesday, February 1 at 8 a.m., Bradley Brim, product engineer, and Sam Chitwood, product engineer
- **Achieving Double Data Rates with Forward Error Correction Encoding—** Wednesday, February 1 at 10 a.m., Mehdi Mechaik, senior application engineer, and Daniel Dreps, DE design engineer, IBM
- **Panel: Are Eye Diagrams Obsolete?—**Wednesday, February 1 at 3 p.m., Kumar Keshevan, senior software architect
- **Using Automated IBIS-AMI Modeling Tools to Model Advanced SerDes IP—** Thursday, February 2 at 8:30 a.m., Jared James, principal product engineer, Ambrish Varma, senior principal software engineer and Ken Willis, product engineering director
- **A Practical Simulation Solution for System-Level ESD Analysis—**Thursday, February 2 at 9:20 a.m., Zhen Mu, senior principal product engineer

- **LPDDR4 Signal Integrity Design Optimization Techniques for Developing Higher Quality Mobile Products—**Thursday, February 2 at 10:15 a.m., Kumar Keshavan, senior software architect, Ambrish Varma, senior principal software engineer and Ken Willis, product engineering director
- **Heterogeneous System-Level Integration Driven from the Virtuoso® Platform—** Thursday, February 2 at11:05 a.m. and 3:45 p.m., John Park, product management director
- **Enabling Accurate and Efficient 3D Full-Wave Extraction for Both 3D Experts and Non-Experts—**Thursday, February 2 at 2 p.m., Bradley Brim, product engineering architect
- **Efficient On-Chip 3D Electromagnetic Modeling Driven from the Virtuoso Environment—**Thursday, February 2 at 2:50 p.m., Michael Brenneman, senior principal software engineer

In addition, the following demonstrations will be displayed in the Cadence booth:

- Constraint-driven power integrity design and analysis featuring easy setup with automated model and source/sink assignments
- Power-aware simulation and rule checks for DDR4 memory interface design and analysis
- Multi-gigabit serial link design and analysis featuring compliance testing for popular interfaces such as PCI Express® (PCIe®) 4.0
- Trends in advanced IC packaging
- Update on PCIe 4.0 controller and PHY bring-up and interoperability

WHEN: DesignCon is scheduled for January 31 – February 2, 2017.

WHERE: Santa Clara Convention Center in Santa Clara, Calif. Cadence is located in booth 515.

About Cadence

Cadence enables global electronic design innovation and plays an essential role in the creation of

today's integrated circuits and electronics. Customers use Cadence software, hardware, IP and services to design and verify advanced semiconductors, consumer electronics, networking and telecommunications equipment, and computer systems. The company is headquartered in San Jose, Calif., with sales offices, design centers and research facilities around the world to serve the global electronics industry. More information about the company, its products and its services is available at www.cadence.com.

About DesignCon

DesignCon is the world's premier conference for chip, board, and systems design engineers in the high-speed communications and semiconductor communities. DesignCon, created by engineers for engineers, takes place annually in Silicon Valley and remains the largest gathering of chip, board, and systems designers in the country. This three-day technical conference and expo combines technical paper sessions, tutorials, industry panels, product demos and exhibits from the industry's leading experts and solutions providers. More information is available at: designcon.com. DesignCon is organized by UBM Americas, a part of UBM plc (UBM.L), an Events First marketing and communications services business. For more information, visit ubmamericas.com.

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